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Material innovation toward three-dimensional brain-mimicking integrated circuit

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Abstarct

Over past 19 years, the transistor size decreases 26 times from 130 to 5 nm. Unfortunately, the operation speed of the most advanced microprocessor increases only slightly from 1.5 GHz to 3 GHz, although the device downscaling will soon reach the quantum-mechanical limit within half decade. To improve the crucial operation speed, multicore microprocessor has been implemented, but the consumed power increases with number of cores. The power consumptions are vital for cloud compeering, which has wasted >1% global electricity. The projected electricity consumption by electronics will increase monotonically with time. Stephen Hawking warned repeatedly that Earth could be doomed by human beings before we get burned on Earth at year 2600. To address these problems, we pioneered the Three-Dimensional (3D) Integrated Circuit (IC) and published in prestigious “Intl Electron Devices Meeting” (IEDM) in 2004. The 3D IC is the enabling technology to improve the power consumption, speed, transistor density, cost, and performance gap to bio system. The 3D IC chip was already realized in Apple’s A7 microprocessor using die stacking technology, but the too low interconnect density is limited by the basic material property. To further improve the performance of 3D IC toward brain-mimicking function, we initiated the Monolithic 3D IC architecture, which was realized by integrating high-mobility nano-crystal materials to standard MOS transistors on the backend inter-metal-dielectric amorphous-SiOx layers of IC chips. The monolithic 3D IC provides >106 times higher interconnect density than present die stacking 3D IC, the key technology to enable electronic neurons and brain-mimicking IC.

Biography

Albert Chin received Ph.D. from university of michigan. He was with AT&T bell labs, GE electronic-lab, and TI SPDC. He is a pioneer on high-κ CMOS, high-κ flash memory, and 3D IC. He co-authored >500 papers (h-index=55), three “top 100 scientific reports physics papers” in 2017~2019, one “top articles in device physics of applied physics letters”. He has served as IEDM executive committee, editor of IEEE electron device letters, technical committee chairs on “electronic materials” and “compound semiconductor devices & circuits”. He is a IEEE Fellow, The optical society fellow, and asia pacific academy of materials academician.

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